BUMPLESS FLIP CHIP ASSEMBLY WITH SOLDER VIA

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is continuation of U.S. application number 09/465,024 filed on December 16, 1999, which is an application filed in accordance with 35 U.S.C. §119 and claims the benefit of earlier filed Singapore application number 9804817-6 filed on December 17, 1998.

1. Field of the Invention

This invention relates generally to a semiconductor device assembly, and in particular, relates to a connection of integrated circuit (IC) chip or chips to substrate circuitry, printed circuit board, and interconnect components.

2. Background of the Invention

Recent developments of semiconductor packaging suggest an increasingly critical role of the technology. New demands are coming from requirements for more leads per chip and hence smaller input/output terminal pad pitch, shrinking die and package footprints, and higher operational frequencies that generate more heat, thus requiring advanced heat dissipation designs. All of these considerations must be met and, as usual, placed in addition to the cost that packaging adds to the overall semiconductor manufacturing costs.

Conventionally, there are three predominant chip-level connection technologies in use for integrated circuits, namely wire bonding, tape automated bonding (TAB) and flip chip (FC) to electrically or mechanically connect integrated circuits to leadframe or substrate circuitry. Wire bonding has been the far most broadly applied technique in the semiconductor industry because of its maturity and cost effectiveness. However, this process can be performed only one wire bond at a time between the semiconductor chip's bonding pads and the appropriate interconnect points. Furthermore, because of the ever increasing operational frequency of the device, the length of the interconnects needs to be shorter to minimize inductive noise in power and ground, and also to minimize crosstalk between the signal leads. An example of such a method is disclosed in U.S. Pat. No. 5,397,921 issued to Karnezos.

Flip chip technology is characterized by mounting of the unpackaged semiconductor chip with the active side facing down to an interconnect substrate through contact anchors such as solder, gold or organic conductive adhesive bumps. The major